REMARKS

The final Office Action of November 27, 2002 was received and carefully reviewed. The Applicants wish to thank the Examiner for the courtesies extended during the telephone interview of January 21, 2003. In light of the interview, the Applicants present the amendments to claim 1 above, which find support in the specification at least at Figures 2-6, elements 3, 7, 9, 11a, 12a and page 20, lines 7-25, as well as Figures 10-12, elements 21, 7, 9, 11a, 12a, and page 42, lines 8-25. For the reasons advanced in detail below, reconsideration and withdrawal of the currently pending rejection is requested. Claims 1-12 remain pending.

With regard to the Examiner's rejection of claims 1-12, under 35 U.S.C. 103(a), as being obvious in view of the teachings of the Applicants' admitted prior art (APA) at Figures 14-18 combined with the teachings of Satoh '374, this rejection is respectfully traversed.

Specifically, in response to this rejection, the Applicants have reviewed specification and original claim 1 and determined that an obvious error was set forth in each, which has been corrected by the above amendment. The Applicants are of the opinion that this obvious error has resulted in the Examiner setting forth the above rejection under 103, which would now be overcome upon making the above corrections to provide consistency with the remaining portions of the specification.

Summary of the Invention

As pointed out in the Applicants' Response of September 27, 2002, the presently claimed invention is directed generally:

> to a semiconductor device with a high breakdown voltage comprising a semiconductor substrate of a first conductivity type, a drain region of a second conductivity type, a metal electrode electrically connected to the

> drain region, and an interlevel dielectric film formed **over a gate insulating film, a field insulating film and a plurality of plate electrodes**. In accordance with claims 1-12, parts of the metal electrode are **extended onto an interlevel dielectric film and located over the plate electrodes**. (emphasis added)

These features of the invention are disclosed in the specification, Figures 2-6, elements 3, 7, 9, 11a, 12a, 15-1, 15-2, and page 20, lines 7-25, as well as Figures 10-12, elements 21, 7, 9, 11a, 12a, 15-1, 15-2, and page 42, lines 8-25, as the only manner of forming the metal electrodes onto the interlevel dielectric and over the plate electrodes which are formed under the interlevel dielectric.

However, a review of the specification, at page 13, lines 22-24, and original claim 1 reveals that instead of setting forth the sole disclosed manner of forming the metal electrodes onto the interlevel dielectric and over the plate electrodes which are positioned under the interlevel dielectric, each instead mistakenly sets forth the limitations:

> "And the interlevel dielectric is formed **over** the gate insulating film and the field insulating film and **under** the plate electrodes. The device is characterized in that parts of the metal electrodes are extended onto the interlevel dielectric film and located **over** the respective plate electrodes and that is capacitively coupled to an associated one of the plate electrodes." (Emphasis added)

and

> "an interlevel dielectric film formed **over** the gate insulating film and the field insulating film and **under** the **[floating] plate electrodes**, wherein parts of the metal electrode are extended onto the interlevel dielectric film and are located over the **[floating] plate electrodes**, .." (Emphasis and antecedent basis added)

that are at best confusing and indefinite and at worst wholly unsupported by the remaining description of the invention, including the admitted prior art.

The admitted prior art, at Figures 14-18 and page 2, lines 5-19, explicitly states that the element 11b is a "floating plate electrode"; while also referring to element 12b as

a "plate electrode" and still further referring to elements 16 17 as "floating electrodes." Additionally, the description of the invention at least at page 20, line 17-21, refers to elements 11a and 12a as "plate electrodes" that are "floating."

Further, reference is made to MPEP Chapters 2111-2112 which explicitly require the Examiner to look to the Applicants' specification for the definition or "broadest reasonable interpretation" of the claimed terms, i.e., "floating plate electrodes" or "plate electrode." Therefore, in evaluating the above noted terms of the original claim 1, the terms "floating plate electrodes" and later "plate electrodes" must be viewed by the Examiner as those elements defined at least at Figures 2-6, elements 3, 7, 9, 11a, 12a, 15-1, 15-2, and page 20, lines 7-25, as well as Figures 10-12, elements 21, 7, 9, 11a, 12a, 15-1, 15-2, and page 42, lines 8-25. In performing this evaluation, the limitation of original claim:

> "an interlevel dielectric film formed **over** the gate insulating film and the field insulating film and **under** the **plate electrodes**, wherein parts of the metal electrode are extended onto the interlevel dielectric film and are located **over** the **plate electrodes**, .." Emphasis added

would be confusing since the "plate electrodes" of the invention description, i.e., elements 11a, 12a, have the interlevel dielectric film deposited thereon and not beneath the "plate electrodes"

Therefore, the Applicants' amendments to claim 1 clarify the invention by reducing the (clarity and support) issues for appeal by limiting the invention to the only manner of depositing the interlevel dielectric film and metal electrode taught by the description of the invention. Further, such an amendment would not necessitate a further search or consideration since the Examiner, in outlining a search, must rely upon the Applicants' description/definition of the claim terms, "floating plate electrodes" and "plate electrodes," pursuant to MPEP Chapters 2111 and 2112.

In light of the discussion above, entry and consideration of the amendments is respectfully requested.

Rejection under 35 U.S.C. 103(a) over the APA and Satoh '374

Turning to the Examiner's §103 rejection of claims 1-12, the above amendments to the claim 1 effectively remove the Applicants' admitted prior art (APA), evidenced by Figure 14-18, since the APA does not teach or suggest the claimed highlighted limitations:

> a metal electrode electrically connected to the drain region;
>
> a plurality of electrically floating plate electrodes, which are spaced apart from, and surround, the drain region when the device is viewed from over the substrate; and
>
> an interlevel dielectric film formed over the gate insulating film, the field insulating film and the floating plate electrodes,
>
> wherein parts of the metal electrode are extended onto the interlevel dielectric film and are located over the floating plate electrodes, and
>
> wherein each said part of the metal electrode is capacitively coupled to an associated one of the floating plate electrodes.

That is, the floating plate electrode 16, 17 of the APA are capacitively coupled to the floating plate electrodes 11b, 12b; while the metal electrode 15 connected to the drain is also connected to the plate electrode 12b, see page 2, lines 5-7. The parts of the metal electrode 15 extending above the plate electrode 12b of the APA are not capacitively coupled to plate electrode 12b. Such a structure is distinctly different from that presently claimed where the metal electrode parts are extended onto the interlevel dielectric film and are located over the floating plate electrodes and each said part of the metal electrode is capacitively coupled to an associated one of the floating plate electrodes.

The Satoh '374 reference does not remedy this deficiency, since the APA (and the claims 1-12) relates to a semiconductor device with a high breakdown voltage, while

Satoh is directed to a low voltage (<20V) nonvolatile semiconductor memory device. Again, the Examiner must, according to MPEP Chapter 2112, rely upon the broadest reasonable interpretation of the claimed term "Semiconductor device with a high breakdown voltage..." taught by the specification. The specification, at page 4, lines 12-16; page 6, lines 13-23; page 7, lines 12-22, provides an explicit definition of the "Semiconductor device with a high breakdown voltage..." of the APA, and also provides an explicit definition, at page 18, lines 19-21, of the "Semiconductor device with a high breakdown voltage..." of claims 1-12. In other words, the APA and Satoh are directed to totally incompatible semiconductor devices.

Further, the portion of Satoh (Figure 5A, elements 14, 16), relied upon by the Examiner, discusses the positioning and capacitive coupling of two "gate" electrodes (column 9, lines 26-35), like the APA, and not the capacitive coupling of a "floating plate electrode" and the "parts" of metal electrode connected to a drain as presently claimed. Hence, not only does Satoh, upon being combined with the APA, fail to teach each feature of the now claimed invention, but the low voltage memory device teachings of Satoh also provide no motivation for modifying the high voltage semiconductor device of the APA such that the "floating (plate) electrodes" 16 and 17 are removed and replaced with the overlying parts of metal drain electrode 15 that are capacitively coupled to the floating plate electrodes 11b and 12b. Therefore, one having ordinary skill in the art would not look to Satoh when seeking to modify the alleged APA.

For the above reasons, the Applicants urge that the rejection of claims 1-12, under §103(a), based upon the combined teachings of the APA and Satoh does not establish a *prima facie* case of obviousness based upon the criteria outlined in MPEP Chapter 2143, and respectfully request withdrawal of the §103(a) rejection.

Conclusion

Accordingly, Applicant respectfully contends that the claimed invention defines subject matter that is clearly patentably distinct over the prior art of record. It is respectfully requested that the rejection be withdrawn. If the Examiner believes further discussions with Applicants' representative would be beneficial in this case, he is invited to contact the undersigned.

Respectfully submitted,

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Version with Markings to Show changes Made

In the Specification:

Please replace the paragraph spanning pages 13 and 14, beginning "An inventive high-voltage..." with the following:

-- An inventive high-voltage semiconductor device includes:

semiconductor substrate of a first conductivity type; semiconductor region of a second conductivity type; source and drain regions of the second conductivity type; body region of the first conductivity type; gate insulating film; gate electrode; field insulating film; metal electrode; plate electrodes; and interlevel dielectric film. The semiconductor region is defined in the substrate. The drain region is defined approximately at the center of the semiconductor region. The body region is defined in the semiconductor region so as to be spaced apart from, and to surround, the drain region. The source region is defined in the body region. The gate insulating film is deposited over the body region. The gate electrode is formed on the gate insulating film. The field insulating film is deposited over a part of the semiconductor region between the body and drain regions. The metal electrode is electrically connected to the drain region. The plate electrodes are in an electrically floating plate state, and are spaced apart from, and surround, the drain region when the device is viewed from over the substrate. And the interlevel dielectric film is formed over the gate insulating film, [and] the field insulating film and [under] the plate electrodes. This device is characterized in that parts of the metal electrode are extended onto the interlevel dielectric film and located over the respective plate electrodes and that each said part of the metal electrode is capacitively coupled to an associated one of the plate electrodes. - -

In the Claims:

Please amend claim 1 as follows:

1. (Amended) A semiconductor device with a high breakdown voltage, comprising :

a semiconductor substrate of a first conductivity type;

a semiconductor region of a second conductivity type, which is defined in the substrate;

a drain region of the second conductivity type, which is defined approximately at the center of the semiconductor region;

a body region of the first conductivity type, which is defined in the semiconductor region so as to be spaced apart from, and to surround, the drain region;

a source region of the second conductivity type, which is defined in the body region;

a gate insulating film deposited over the body region;

a gate electrode formed on the gate insulating film;

a field insulating film deposited over a part of the semiconductor region, the part being located between the body and drain regions;

a metal electrode electrically connected to the drain region;

a plurality of electrically floating plate electrodes, which are spaced apart from, and surround, the drain region when the device is viewed from over the substrate; and

an interlevel dielectric film formed over the gate insulating film, [and] the field insulating film and [under] the floating plate electrodes,

wherein parts of the metal electrode are extended onto the interlevel dielectric film and are located over the floating plate electrodes, and

wherein each said part of the metal electrode is capacitively coupled to an associated one of the floating plate electrodes.